Remarks

Claims 1-12 are pending in the present application. By this paper, Applicants have canceled claims 1-12 and added claims 13-24 to more clearly define the invention. The applicant respectfully submits that the new claims are supported by the originally filed specification. Additionally, Applicant has amended the specification by replacing it with a substitute specification under 37 C.F.R. §1.125. No new matter has been added to the specification.

Anticipation Rejection

The Examiner has rejected claims 1-12 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,905,277, issued to Nakamura (hereinafter "*Nakamura*"). Applicant has cancelled claims 1-12 and replaced them with new claims 13-24. To the extent the §102(b) rejection relates to new claims 13-24, Applicants respectfully traverse.

In order to anticipate a claim, a reference must teach each and every element of that claim. Because *Nakamura* falls short of this standard, as will be explained below, the anticipation rejection should be withdrawn. It should be noted that *Nakamura* refers to a method for enciphering and deciphering instructions in a microcomputer, whereas the present invention, on the other hand, refers to a method for transforming data (e.g. messages).

Claim 13

With regard to claim 13, *Nakamura* fails to teach "determining a number (n) of cycles for transformation of initial data under a predetermined criterion." Rather, *Nakamura* merely discloses that ROM is accessed by address signals generated from a program counter (col. 2, lines 35-36). The *Nakamura* counter counts the command number from the succession of commands (instruction code), but does not determine the number of commands. The present application, in contrast, refers to cyclic repetition of operations of transformation of initial

data, wherein the number of cycles is determined under a predetermined criterion, e.g. by limiting the amount of transformed data (C_i).

Moreover, *Nakamura* fails to teach "generating a random number (R_i) which determines a characteristic function used for transformation of the data in the current transformation cycle (i)." Rather, *Nakamura* merely discloses a control circuit used for providing an output control signal (col. 2, lines 44, 51-53).

Further, *Nakamura* does not teach "transforming the data using the selected characteristic function" and "repeating cycle (i) for transformation the number (n) times." *Nakamura* discloses a counter that determines the succession of commands (instruction code) but *not* the number of cycles of transformation of initial data. In that regard, *Nakamura* does not refer to cyclic recurrence of transformation operations at all.

Further yet, *Nakamura* does not teach "forming a cycle data (C_i) and an accessory data (F_i) as a result of transformation of the initial data in each cycle." Rather, *Nakamura* discloses a discriminating circuit that is used for the generation of a control command of a signal for selection of one of two instruction decoders 5 or 6. In the present application, on the other hand, the accessory data (F_i) formed is part of the encoded data, and the cycle data (C_i) formed is the initial data for the next transformation cycle. Accordingly, the discriminating circuit of *Nakamura* does not perform the recited step.

Finally, *Nakamura* fails to teach "forming an encoded data having two parts, wherein the first part includes a finally transformed data (C_n) and the second part includes and accessory data array ($F = \{F_1, F_2, \ldots, F_n\}$)." *Nakamura* merely discloses that instruction codes can be coded in one predetermined coding format and another predetermined coding format. According to the Examiner, one predetermined format is equivalent to (C_n) and another coding format is equivalent to (F). On the contrary, the "one predetermined format" and the "another predetermined format" in *Nakamura* are different forms for providing the same information. In the present application, however, (C_n) and array ($F = \{F_1, F_2, \ldots, F_n\}$) are different

information. That is, both parts, (C_n) and ($F = \{F_1, F_2, \ldots, F_n\}$), are encoded data. Without one of the parts, (C_n) or ($F = \{F_1, F_2, \ldots, F_n\}$), decoding is impossible.

<u>Claims 14-18</u>

Claims 14-18 are dependant claims and are believed to be allowable based upon their dependency from an allowable independent claim. However, Applicants believe these claims recite additional features that distinguish them from *Nakamura*. In that regard, claim 14 recites the additional feature "wherein the length of the cycle data (C_i) is shorter than or equal to the length of the initial data, the predetermined criterion determines the length of the finally transformed data (C_n), and the length of the finally transformed data (C_n) is shorter than the length of the initial data." *Nakamura* fails to disclose this limitation. Rather, *Nakamura* teaches that a predetermined bit in address is used, which is part of the deciphering apparatus (see also col. 2, lines 56 - 57), whereas in the present application the cycle data (C_i) and the accessory data (F_i) for the said cycle are parts of the encoded message, and thus comprise information about the initial data. Furthermore, during the process of transformation one can observe an effect similar to data compression ((C_i) is shorter than or equal to the length of the initial information).

Similarly, claim 15 recites the additional feature "wherein the length of the cycle data (C_i) is shorter than, equal to, or longer than the length of the initial data, the predetermined criterion determines the length of the finally transformed data (C_n) and/or the degree of protectability of the encoded data, and the length of the finally transformed data (C_n) is shorter than, equal to, or longer than the length of the initial data." Again, *Nakamura* fails to disclose this feature. In particular, *Nakamura* discloses that "[t]he number of FET's 14a or 14b is the same as the number of bits in the data bus 3." (col. 2, lines 65-67.) That is, the number of FET's is predetermined exactly. In contrast, the length of the cycle data (C_i), according to the present application, can be different in each transformation cycle. Moreover, *Nakamura* discloses that a predetermined bit in address is used, which is part of the deciphering apparatus (see also col. 2, lines 56 - 57), whereas in the present application the cycle data (C_i) and the

accessory data (F_i) for the said cycle are part of the encoded message, and thus comprise information about the initial data.

Regarding claim 16, the additional feature "wherein the cycle data (C_i) transformed in the cycle (i) and/or the accessory data (F_i) for the cycle (i) are mixed during at least one transformation cycle" is recited. *Nakamura* fails to anticipate this limitation as well. *Nakamura* refers to program designing from a combination of two types of program codes. In contrast, the present application refers to implication in each or in some transformation cycles of the information (C_i) and/or the accessory information (C_i) for the corresponding cycle. Thereby, (C_i) and (C_i) is different information.

Regarding claims 17 and 18, the additional feature "wherein a certain part of the accessory data (F_i) for the cycle (i) is added to the cycle data (C_i) transformed in the cycle (i) during at least one transformation cycle" is recited. *Nakamura* does not disclose this limitation. *Nakamura* refers to program designing from a combination of two types of program codes. The present application, on the other hand, recites that the certain part of the accessory data (F_i) for the cycle is added to the transformed cycle data (C_i) in each or some transformation cycles.

Claim 19

Independent claim 19 is directed towards a device for encoding data, and includes many elements not taught by *Nakamura*. Thus, it is believed that a rejection of claim 19 would be improper.

Specifically, claim 19 recites "a random number generator, electrically disposed between the decision making unit and the database, for generating a random number (R_i) and outputting the feature (R_i) to the database." *Nakamura* fails to disclose this limitation. Contrary to the Examiner's contention, the accumulator of *Nakamura* is not equivalent to a random number generator, but rather is used instead for the storage of information. In the present application,

however, a random number generator is used for generation of random numbers, which are used as addresses for random transformation functions.

Claim 19 also recites "a transformation unit in electrical communication with the input unit and the database, the transformation unit adapted to transform information during each transformation cycle and output cycle data (C_i) and accessory data (F_i)." Again, this limitation is not taught by *Nakamura*. Rather, *Nakamura* discloses instruction decoders that work in turns, either one or the other, depending on a predetermined bit. In the instant application, the transformation unit carries out a single transformation, resulting in two different types of data, i.e. cycle data (C_i) and accessory data (F_i).

Moreover, claim 19 recites "a storage for transformed information for storing cycle data (C_i) inputted from the transformation unit, the storage for transformed information connected to the decision making unit for communication therewith." The *Nakamura* disclosure fails to anticipate this limitation. In particular, *Nakamura* merely discloses that "the first type instruction codes are stored in odd addresses...and the second type of instruction codes are stored in even addresses" (i.e. different types of command codes are stored in different addresses). (Col. 3, lines 22-24.) In the present application, on the other hand, the storage for transformed information stores cycle data (C_i).

Further, claim 19 recites "a storage for accessory information for storing accessory data (F_i) inputted from the transformation unit into an accessory data array ($F = \{F_1, F_2, \ldots, F_n\}$), the storage for accessory information in electrical communication with the decision making unit for receiving instructions therefrom." Similarly, *Namamura* does not disclose this limitation either. Particularly, *Nakamura* merely discloses that "the first type instruction codes are stored in odd addresses...and the second type of instruction codes are stored in even addresses" (i.e. different types of command codes are stored in different addresses). (Col. 3, lines 22-24.) In the present application, however, a storage for accessory information is provided for accumulation of information in the form of the accessory data array ($F = \{F_1, F_2, \ldots, F_n\}$).

Furthermore, claim 19 recites the following limitation: "a decision making unit in electrical communication with the input unit, the decision making unit adapted for making a decision on termination of the encoding process or on switching to the next cycle of encoding, and for outputting corresponding commands." *Nakamura* fails to disclose this limitation. Rather, *Nakamura* merely discloses a selecting circuit 4 that directs the data from the bus 3 to one of the decoders 5 or 6. (Col. 2, line 37-43.) In the present application, on the other hand, the decision making unit makes the decision on completion of a transformation cycle and synchronizes the performance of the random number generator, which generates the address for the random selection of transformation functions for the next transformation cycle.

Finally, claim 19 also recites "a commutator having an at least one input and an at least one output, the at least one input for receiving instructions from the decision making unit and for receiving cycle data (C_i) from the storage for transformed information, the commutator adapted to output the cycle data (C_i) to the transformation unit unless instructions to terminate the encoding process are received from the decision making unit." The *Nakamura* disclosure fails to meet this limitation as well. Specifically, *Nakamura* merely discloses a selecting circuit 4 that directs the data from the bus 3 to one of the decoders 5 or 6. (Col. 2, lines 37-43.) Regarding the present application, however, the commutator is for commutation of the cycle data (C_i) on entry of the transformation unit (if the transformation cycle is not completed) or entry of the output unit (if the transformation cycle is completed), in accordance with the control signal from the outlet of the decision making unit.

<u>Claim 20</u>

Independent claim 20 is directed towards a method for decoding encoded data based on a number (n) of transformation cycles. In that regard, *Nakamura* fails to teach each and every limitation claim 20. Specifically, *Nakamura* fails to teach "isolating the accessory data (F_i) for the transformation cycle (i) from the accessory data array ($F = \{F_1, F_2, \ldots, F_n\}$)." Instead, *Nakamura* merely discloses that the discriminating circuit isolates differing instructions, rather than differentiating data of different transformation cycles. In the present

application, it is the additional information from different transformation cycles that is isolated from encoded data.

Moreover, claim 20 of the present application additionally recites "recovering the cycle data (C_i), which is transformed in the respective transformation cycle by using the selected characteristic function and the accessory data (F_i) for the transformation cycle (i)." Contrary to the Examiner's contention, *Nakamura* fails to disclose this limitation. In that regard, *Nakamura* merely discloses that each type of command code is enciphered by a corresponding predetermined enciphering format, which is the same all the time. In the present application, on the other hand, cycle data (C_i) is transformed during a cycle in accordance with the accessory data (F_i) by different methods or formats.

Further, claim 20 of the present application additionally recites "deciding between switching to the next transformation cycle or terminating the transformation." Again, *Nakamura* does not teach this limitation. Rather, *Nakamura* merely teaches the existence of a selecting means for selecting a transformation device. However, the present application recites deciding between continuation of a transformation cycle or completing the transformation.

Furthermore, claim 20 additionally recites "using in each transformation cycle (i) a respective part of the accessory data (F_i), wherein recovered data is formed in the respective transformation cycle as a result of transformation with the use of the selected characteristic." Contrary to the Examiner's contention, *Nakamura* does not disclose this step. Rather, *Nakamura* simply teaches that a decoder is selected in accordance with a bit of the command address. In the present application, on the other hand, the selection is made in accordance with a part of the encoded information.

Claims 21-23

Claims 21-23 are dependant claims and are believed to be allowable based upon their dependency from an allowable independent claim. However, Applicants believe these claims recite additional features that distinguish them from *Nakamura*. In that regard, claim 21 recites the additional feature "recovering a current communication, as a result of transformation using the selected characteristic function, in the current transformation cycle, the length of which is larger than or equal to the length of a previous communication resulting from transformation in the previous transformation cycle." *Nakamura* fails to disclose this limitation. Particularly, *Nakamura* does not teach that, as a result of each transformation cycle, the length of the communication can be larger than the length of the communication resulting from transformation in the previous cycle. Thus, during decoding one can observe the reverse effect to data compression.

Similarly, claim 22 recites the additional feature "recovering a current communication, as a result of transformation using the selected characteristic function, in the current transformation cycle, the length of which is larger than, equal to, or smaller than the length of a previous communication resulting from transformation in the previous transformation cycle." *Nakamura* fails to anticipate this limitation. Rather, *Nakamura* merely discloses that "the deciphered results from said at least two instruction decipherers coincide with instruction to be performed by said microcomputer". (Col. 9, lines 6-9.) The present application, on the contrary, teaches that the length of information recovered during a cycle can be different from the length of information recovered in the previous cycle. In sum, *Nakamura* merely refers to coincidence of instructions, whereas the present application refers to different lengths of results of transformation cycles.

Moreover, claim 23 recites the additional feature "wherein the cycle data (C_i) transformed in the respective transformation cycle (i) and/or the accessory data (F_i) for the respective transformation cycle (i) are preliminarily unmixed during at least one transformation cycle." Contrary to the Examiner's contention, this limitation is not anticipated by the *Nakamura* reference. Rather, *Nakamura* merely teaches separate decoding of instructions. The present application, on the other hand, recites that, before the start of each transformation cycle, cycle data (C_i) and accessory data (F_i)

are mixed (i.e. a transfer operation takes place), if (C_i) and (F_i) were mixed up during the corresponding cycle in the encoding process.

Claim 24

Independent claim 24 is directed towards a device for decoding data, and includes numerous elements not taught by *Nakamura*. In that regard, *Namamura* fails to disclose "a storage for accessory information in electrical communication with the input unit, the storage for accessory information adapted to store an accessory data array ($F = \{F_1, F_2, \ldots, F_n\}$)." Rather, *Nakamura* merely discloses the existence of read only memory (ROM), while the present application is directed towards read and write memory, or RAM, for data that is to be decoded.

Similarly, *Nakamura* fails to disclose "a storage for transformed information in electrical communication with the input unit, the storage for transformed information adapted to store cycle data (C_i) corresponding to a transformation cycle (i) of a number (n) of transformation cycles." Rather, *Nakamura* merely discloses the existence of read only memory (ROM), while the present application is directed towards read and write memory, or RAM, for data that is to be decoded.

Moreover, claim 24 additionally recites "a transformation unit in electrical communication with the database, the storage for transformed information and the storage for accessory information, the transformation unit configured for transforming information in each transformation cycle." *Nakamura* does not teach this limitation either. Rather, *Nakamura* discloses that instruction deciphers work in turns, either one or the other, depending on the predetermined bit, the transformation result depending on one variable. On the contrary, in the present application, the transformation unit carries out a single transformation, the transformation result thereby depending on two different variables (C_i) and (F_i).

Further, claim 24 also recites "a decision making unit in electrical communication with the database, the storage for transformed information and the storage for accessory information, the decision making unit adapted for making a decision between termination of the decoding process or

switching to the next transformation cycle of decoding, and for outputting corresponding instructions." *Nakamura* fails to anticipate this limitation. Rather, *Nakamura* discloses a selecting circuit in cooperation with a control unit that selects one of the decoders. In the present application, on the other hand, the decision making unit makes the decision whether the cycle is to be continued or stopped, and depending on this decision controls the commutator by directing cycle data (C_i) to the next transformation cycle or to the output unit.

Furthermore, claim 24 additionally recites "a commutator in communication with the storage for accessory information and adapted to receive instruction from the decision making unit, the commutator configured to output cycle data (C_i) to the transformation unit unless instructions to terminate the decoding process are received from the decision making unit." Likewise, *Nakamura* does not disclose this feature. The data bus in *Nakamura* is not connected to the device output, whereas, in the present application, the commutator directs cycle data (C_i) to the next transformation cycle or to the output unit, in accordance with the signal from the output of the decision making unit.

As shown above, the present invention proposes a device quite different from *Nakamura* as it carries out a two-channel transformation by nature. During decoding, two types of data are generated, (C_n) and ($F = \{F_1, F_2, \ldots, F_n\}$), which are encoded data. Without one of these parts (C_n) or ($F = \{F_1, F_2, \ldots, F_n\}$) decoding is impossible. Thereby, the length of (C_n) and ($F = \{F_1, F_2, \ldots, F_n\}$) depends on the length of the initial information. The length (C_n) can be significantly smaller than the length of the initial information, which corresponds to the compression effect. For identical initial information, an encoded (C_n) and ($F = \{F_1, F_2, \ldots, F_n\}$) message, as a rule, is different each time. This is due to the presence of a generator of random numbers in the device, which provides for the selection of transformation for each encoding cycle.

During decoding the initial information is restored from (C_n) by means of ($F = \{F_1, F_2, \ldots, F_n\}$) by a cyclic method. The completion of the cycle is determined by a decision making unit. In *Nakamura*, on the other hand, instruction codes are encoded/decoded by one of the predetermined formats. Transformation cycles of command codes are not proposed. Each determined type of command codes can be encoded/decoded by only one predetermined

method. According to the present application the same information can be encoded with different transformation results. When decoding, different encoded information can be decoded in identical information.

CONCLUSION

Applicants have made a real and genuine effort to respond to each of the Examiner's rejections. In view of the foregoing, Applicants believe that the pending claims are in condition for allowance, which action is respectfully requested.

A check in the amount of $510.00 is enclosed to cover the Petition fee. Please charge any additional fees or credit any overpayments as a result of the filing of this paper to our Deposit Account No. 02-3978.

Respectfully submitted,

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Date: March 8, 2006

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